The DEPFET Pixel Detector (PXD) for BELLE II

Development of High-Resolution Pixel Detectors and their Use in Science and Society
Bad Honnef, Germany

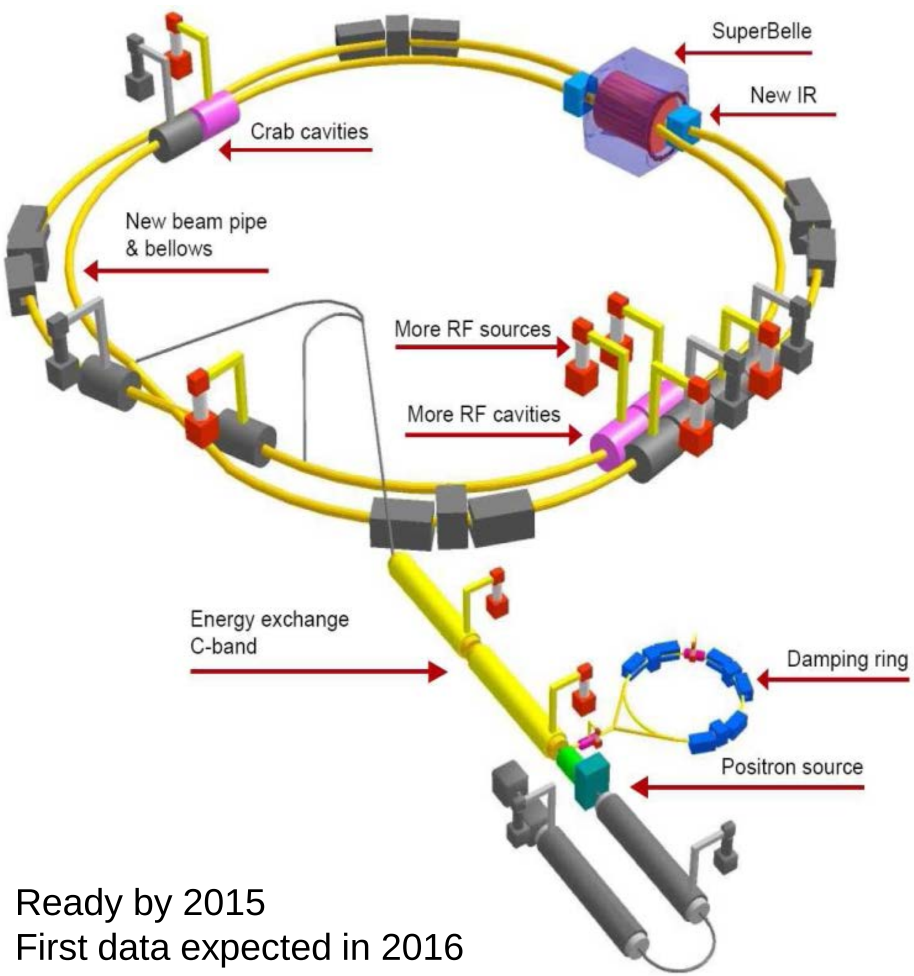
Paola Avella for the DEPFET collaboration

Outline

- SuperKEKB and the BELLE II experiment
- The BELLE II vertex detector
- The DEPFET working principle
- The readout electronics
- DEPFETs for BELLE II technology
- Radiation damages
- Summary

SuperKEKB

Belle-II



Ready by 2015
First data expected in 2016

Use of the same facility of KEKB

with some fundamental **upgrades**

Nano beam scheme
- smaller beam size (~nm)
- Increased beam currents (x2)

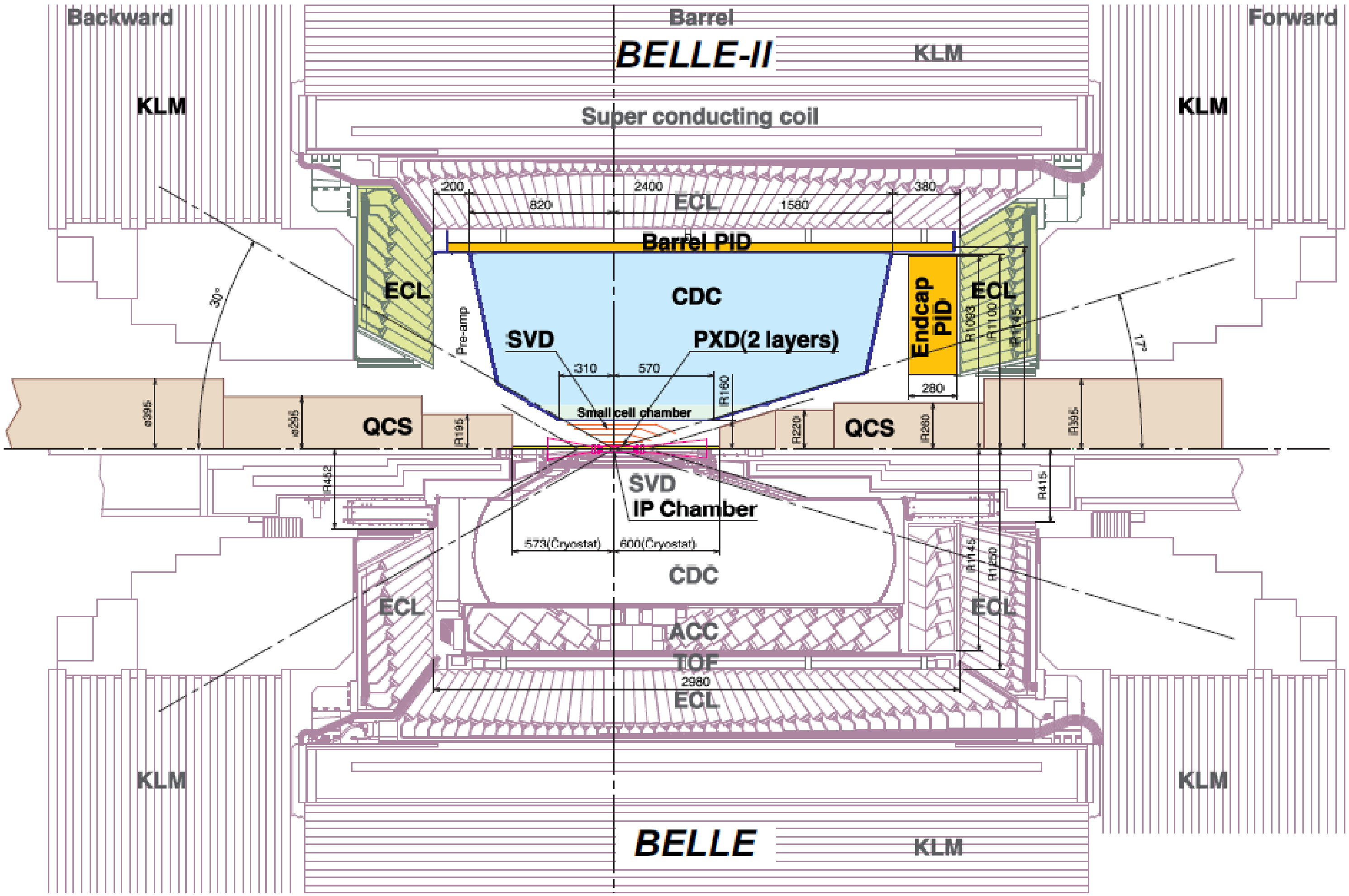
✓ $L = 8 \times 10^{35}$ cm^{-2} s^{-1}

(40 times larger than in KEKB)

✓ $E_{e^-} = 7$ GeV / $E_{e+} = 4$ GeV

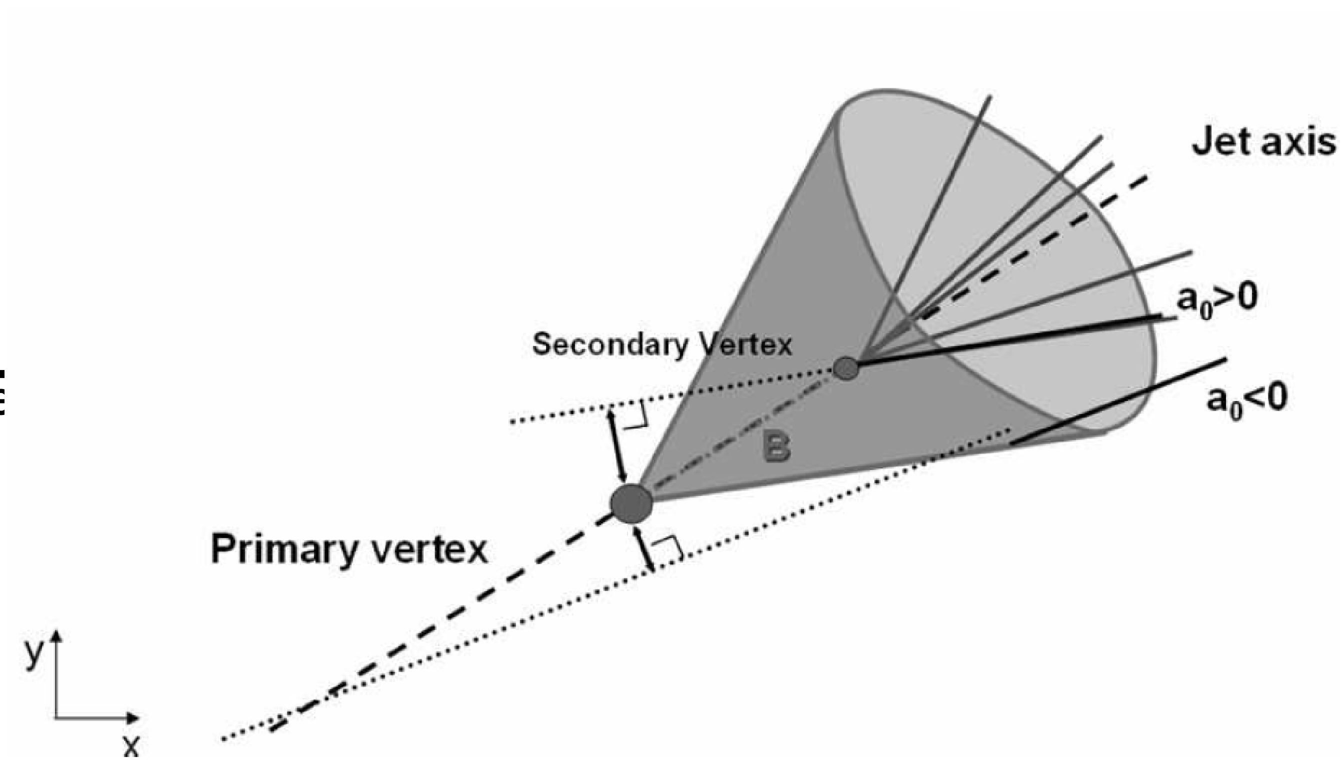
✓ $E_{cm} = 10.58$ GeV – $\Upsilon(4S)$

The BELLE II experiment



BELLE II physics motivation

Measure CP violations.

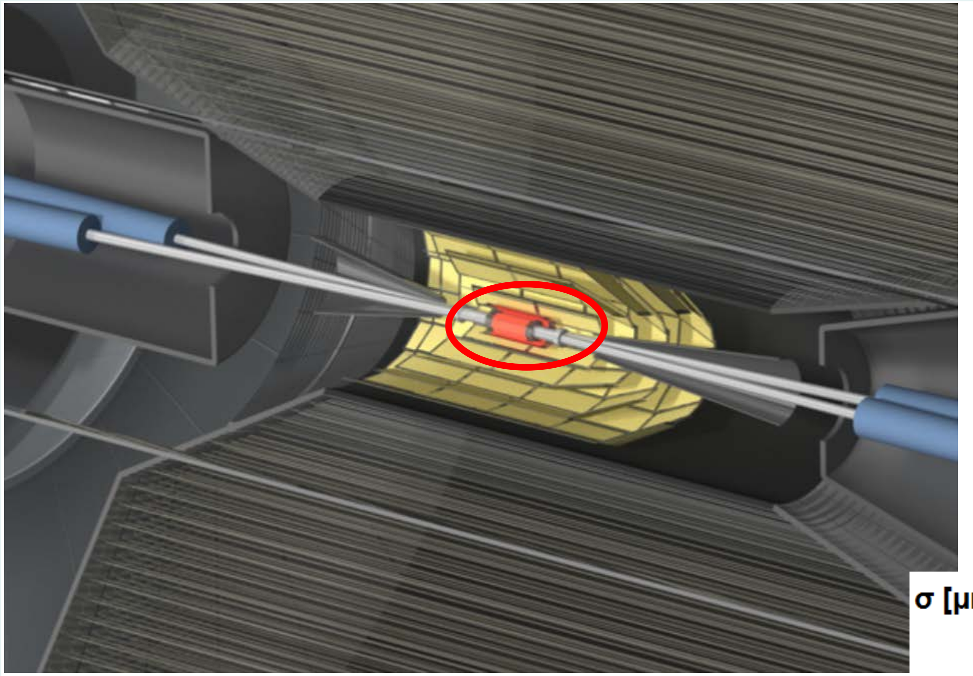


en channel

nnel

The *Lorentz boost* allows measuring decay time differences, difficult to measure, via spatial separation of the vertices.

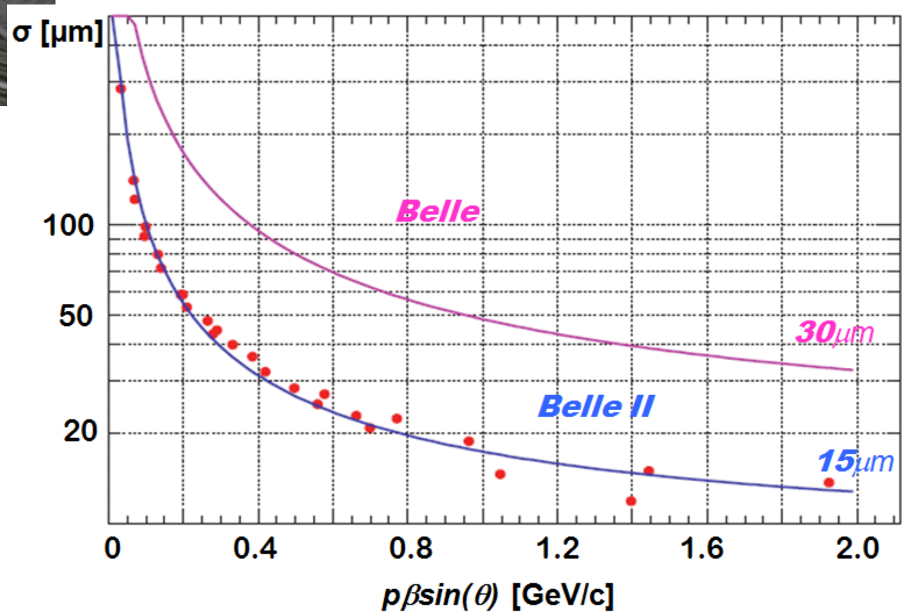
The BELLE II vertex detector



- 2 DEPFET pixel detector (PXD) layers
- 4 Double Sided Si-Strip Detector (DSSD) (SVD) layers

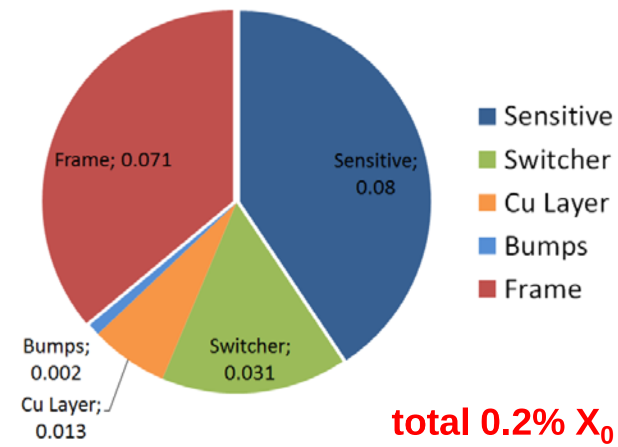
→ *Improvement in the impact parameter resolution*

- Fast detector to keep small occupancy
- High spatial resolution
- Very short distance from the IP
- Minimum thickness

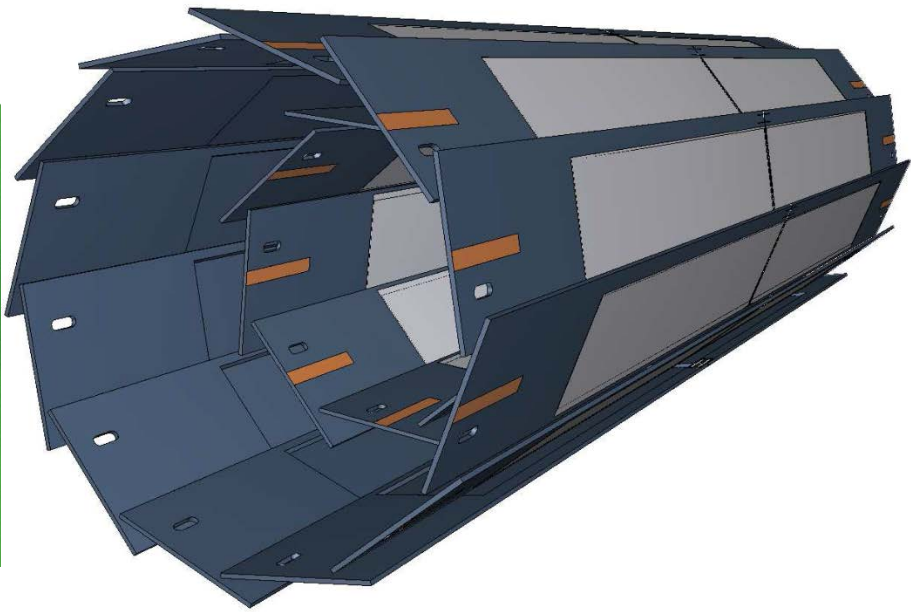


The BELLE II PXD layout

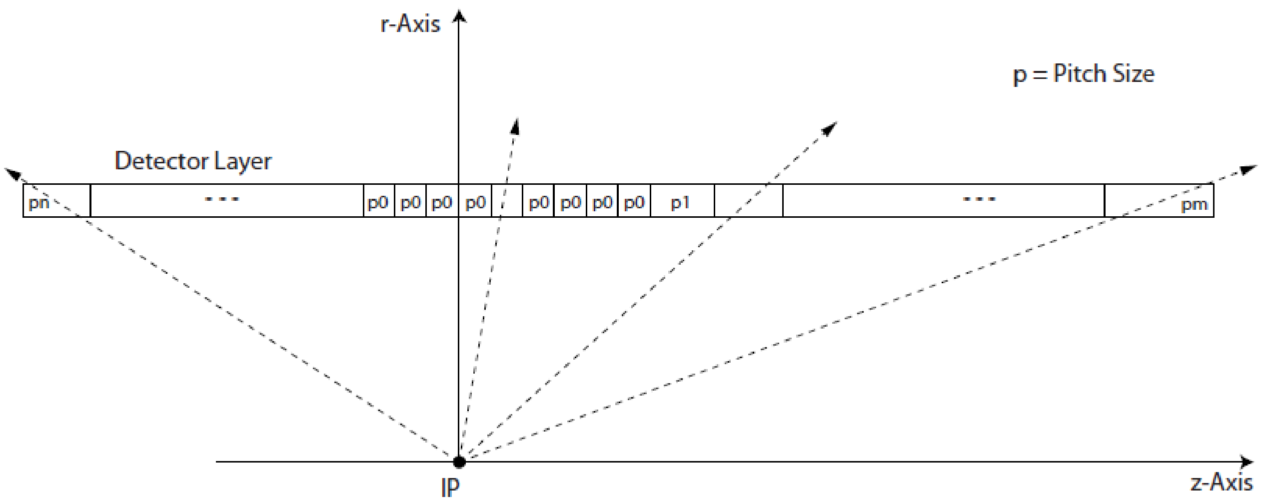
	Inner layer (L1)	Outer layer (L2)
# modules	8	12
Distance from IP (cm)	1.4	2.2
Thickness (μm)	75	75
# pixels	768 x 250	768 x 250
Total # pixels	3.072 M	4.608 M
Pixel size (μm²)	55 x 50 60 x 50	70 x 50 85 x 50
Sensitive area (mm²)	44.8 x 12.5	61.44 x 12.5



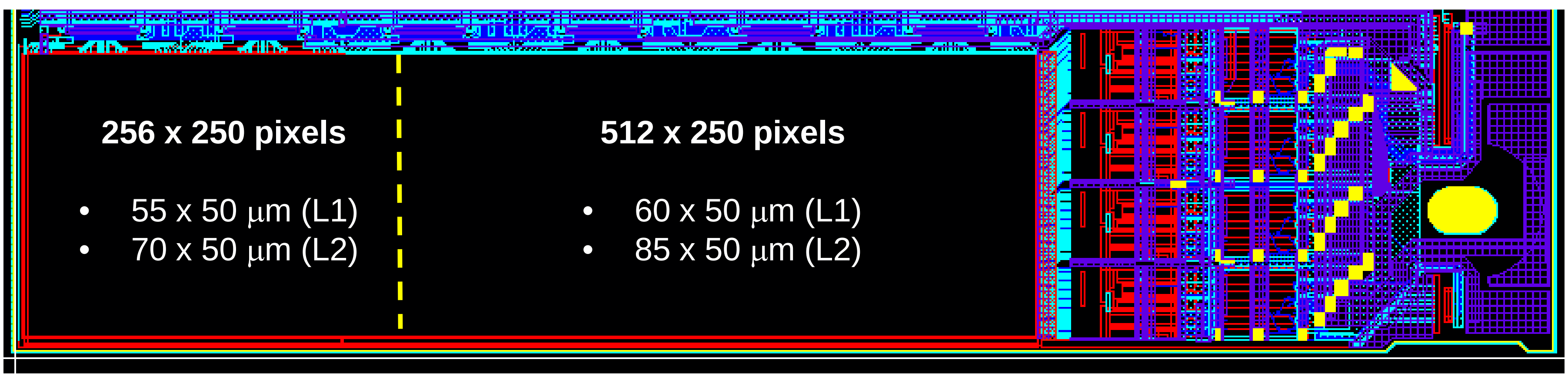
total 0.2% X_0



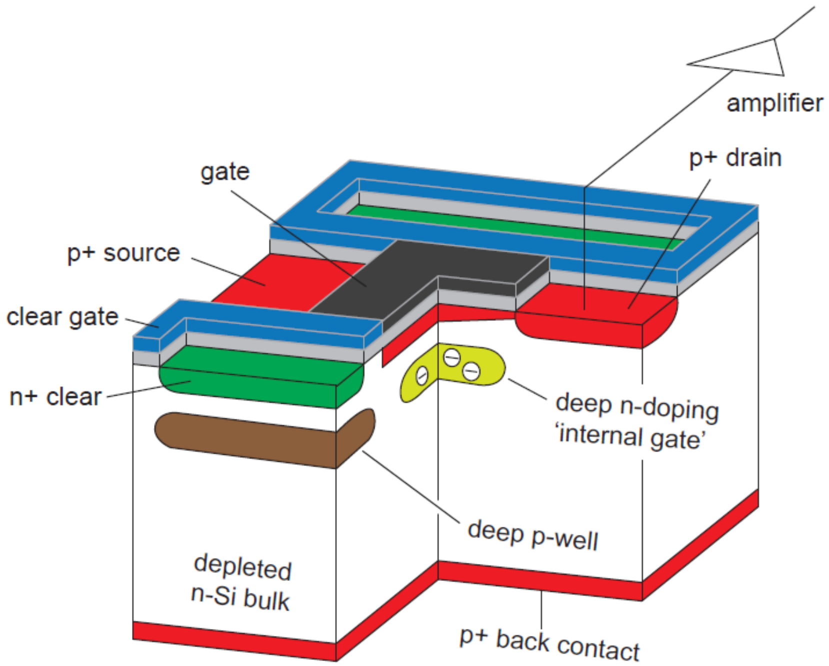
The DEPFET PXD half ladder

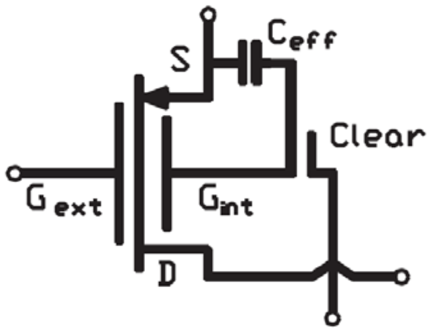


- Decrease of the overall channel readout time
- Charge induced by hits does not spread over too many pixels → better track reconstruction accuracy



The DEPFET working principle

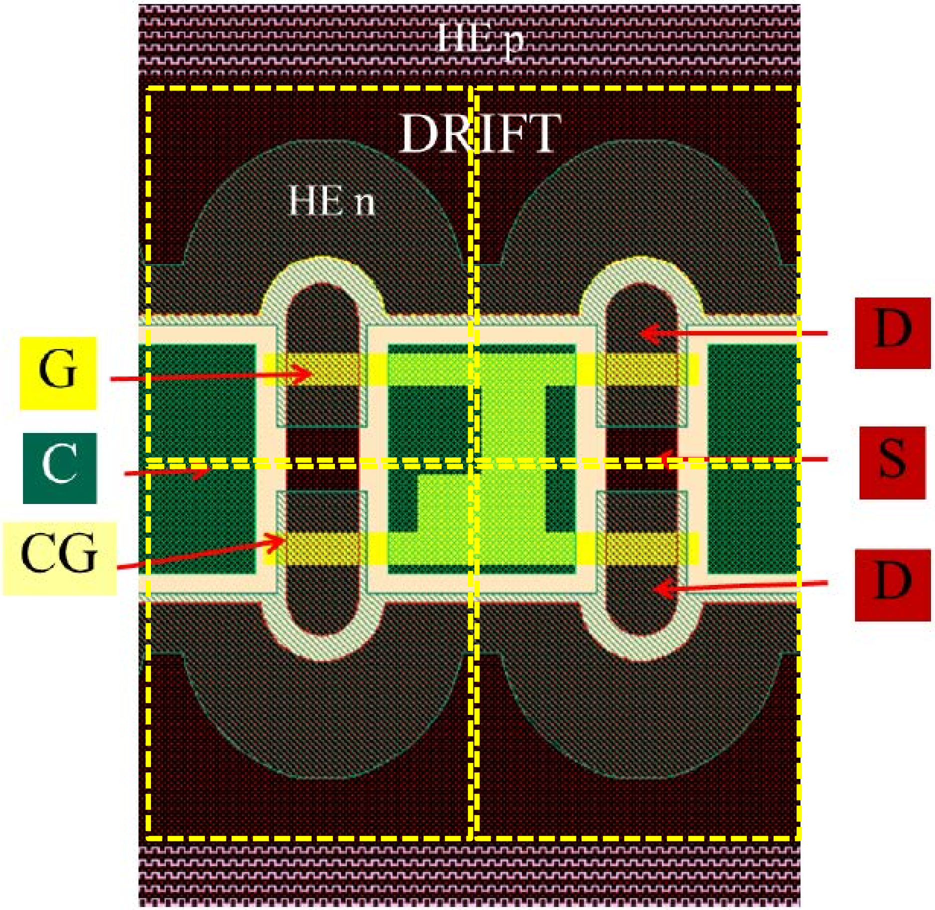




Depleted **p**-channel **FET**

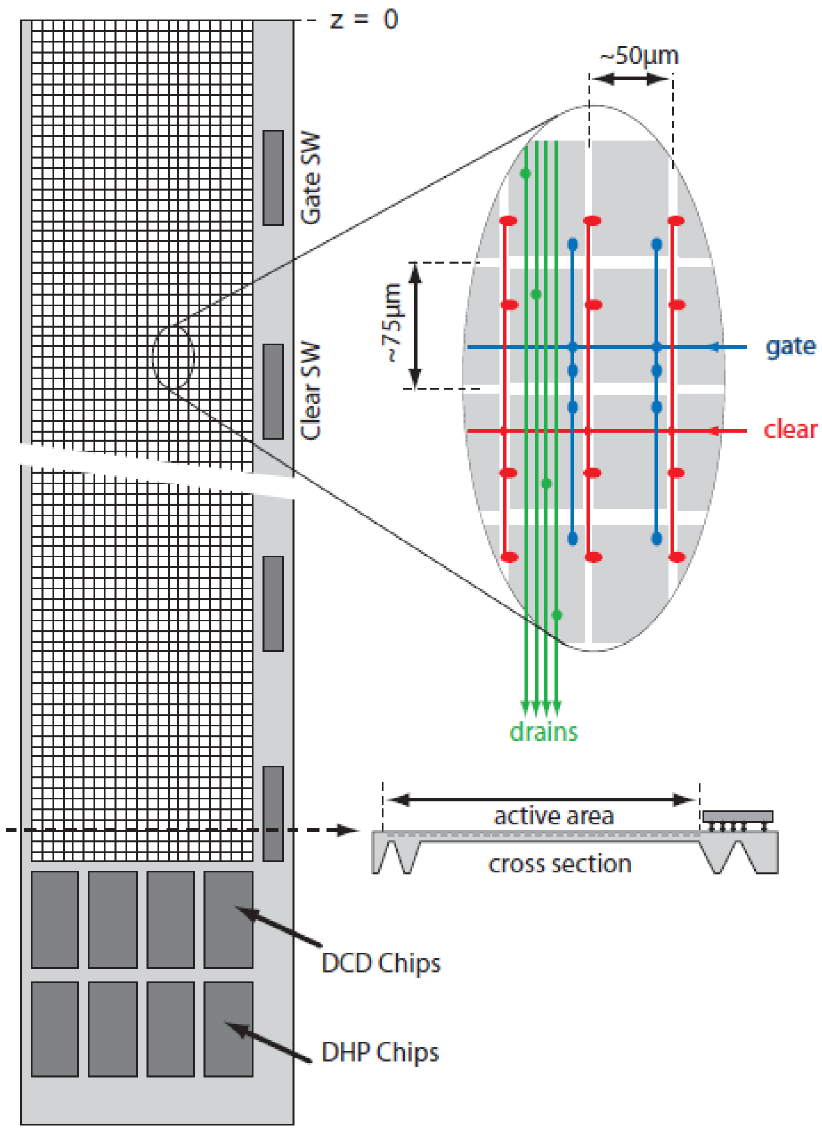
- fully depleted bulk
- potential minimum for electrons
- the charges collected in the internal gate modulate the transistor current
- internal amplification g_q
- non – destructive readout
- low power consumption
- the charge stored in the internal gate is removed by a “reset” contact

The DEPFET pixel



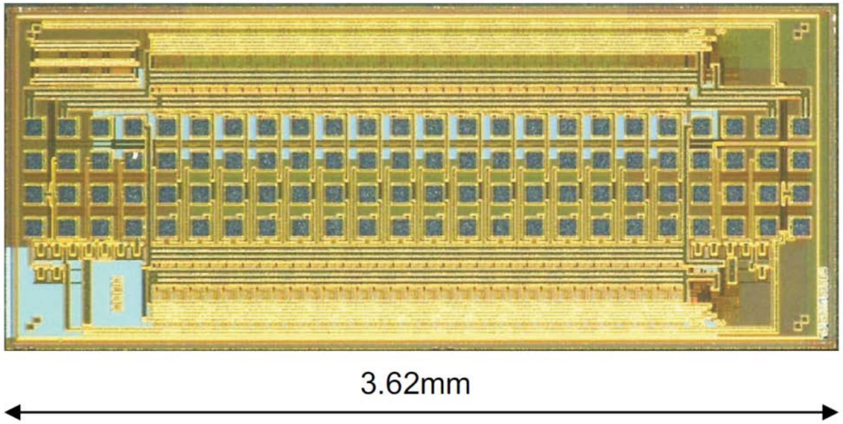
- 25 photolithographic masks and 9 implantations
- Extremely complex technology involving wafer bonding, double poly silicon, triple metal layer, backside thinning and double sided wafer processing
- Source contact common to 2 pixels
- Clear shared by 4 pixels
  → very compact design

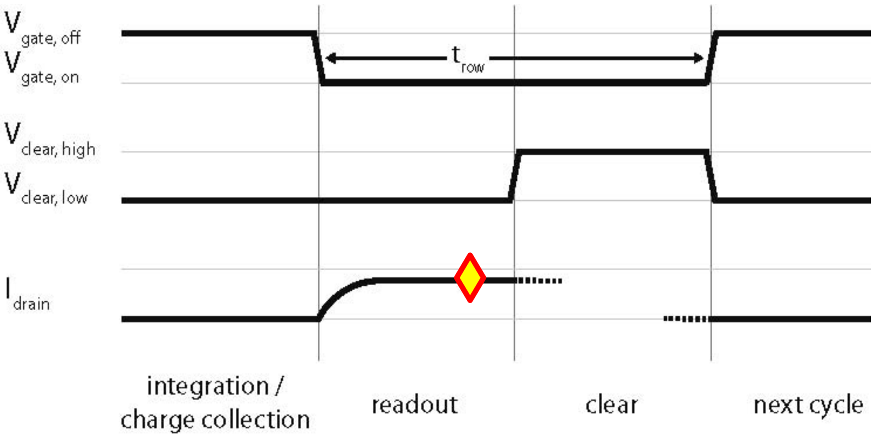
The DEPFET matrix and the rolling shutter mode readout



- High readout speed required to keep the number of hit pixels low at each readout frame → 20 µs → 100 ns/electrical row
- The 4-fold readout is used, for which:
  - 4 rows are connected in parallel to gate and clear
  - The number of drain lines increases of the same factor
- Three different ASICs to readout the matrix (made in radiation hard technology):
  - SWITCHER
  - DCD
  - DHP

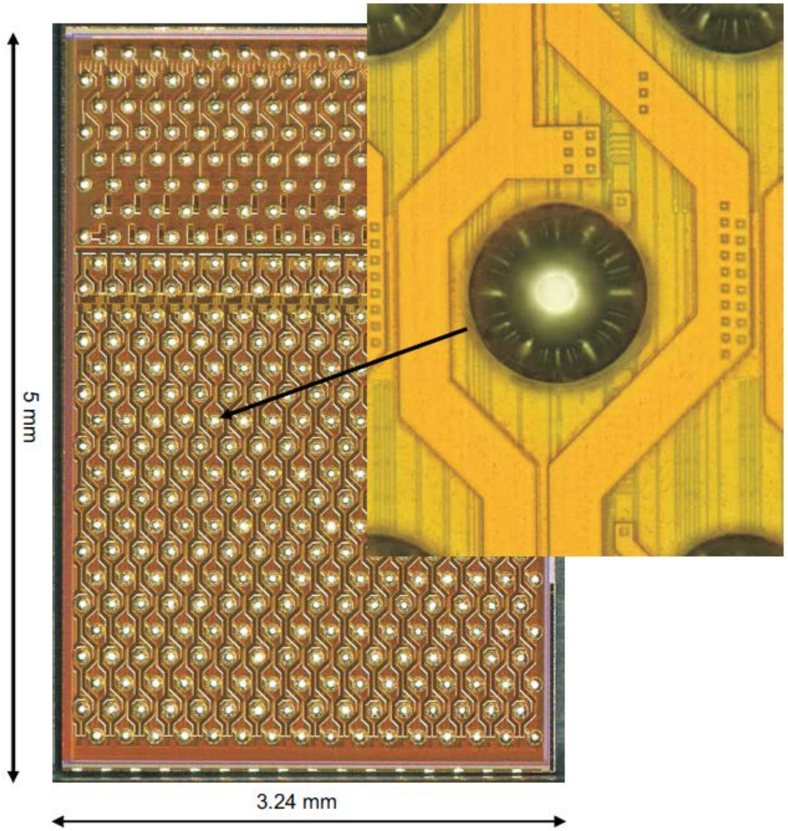
The SWITCHER(18G)





- Mounted on the 2 mm wide and 300 μm thick inactive edge rim of the module
- Provide fast voltage pulses up to 20 V to activate gate rows and to clear the internal gate
- Support gated mode operation
- equipped with JTAG for configuration and debugging
- Each chip has 64 drivers for both gate and clear channels → address 32 matrix segments
- 768 rows → 192 electrical rows → 6 ASICs needed per module

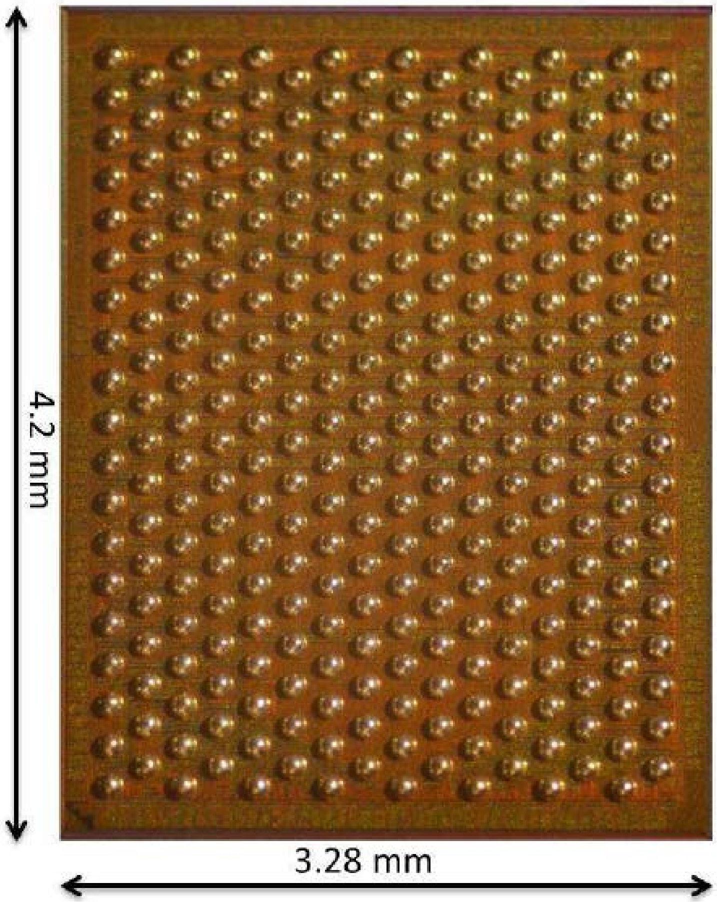
The Drain Current Digitizer (DCD)



- 256 analog channels with **1 input** and **2x8 bits output ADCs** that are interleaved
  → 4 DCDs/half module to readout 1000 pixels

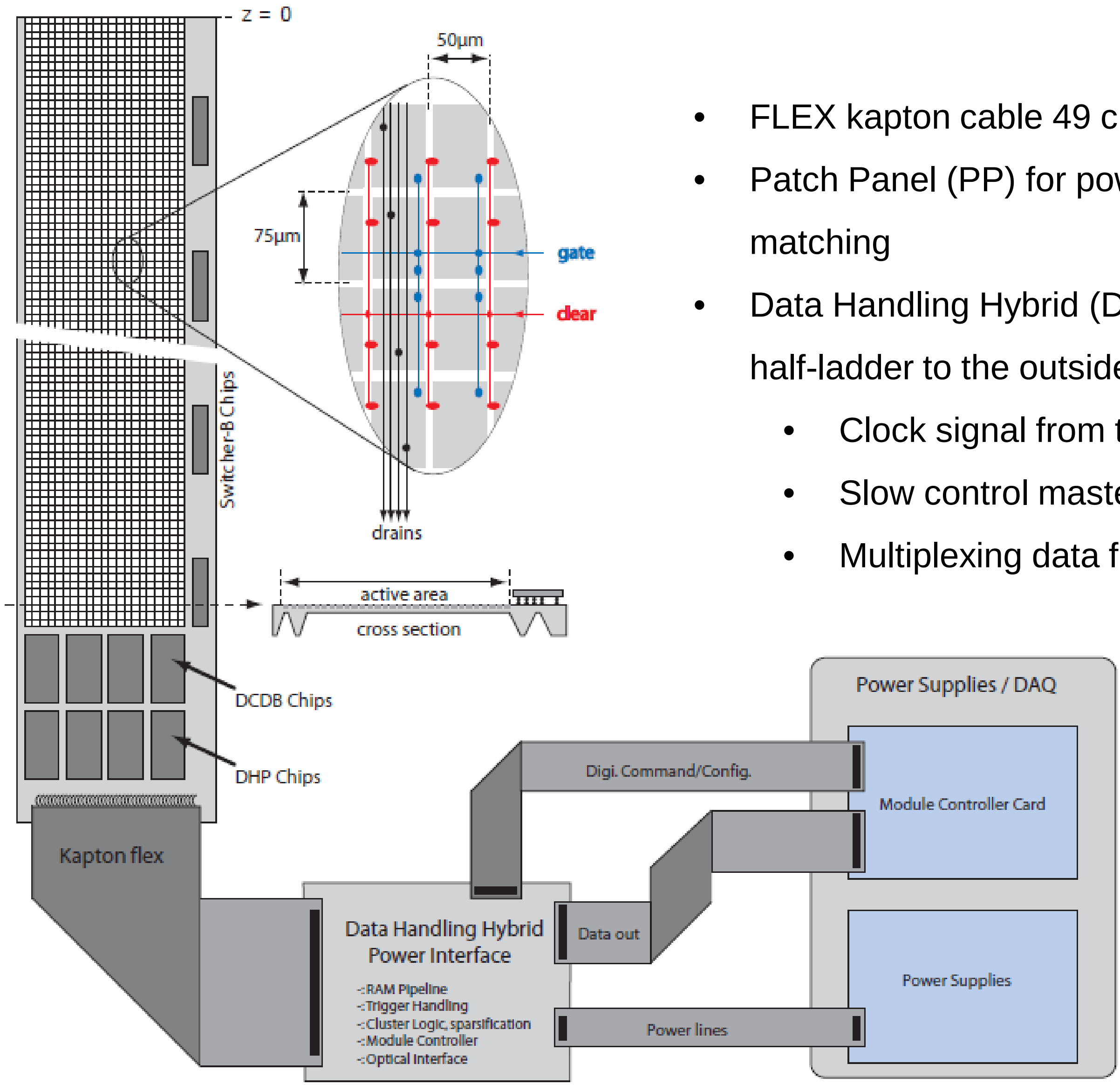
- Tasks of the analog inputs:
  - Keeps the columns line potential constant
  - Compensate for pedestal current variation
  - Amplify the signal
  - Shaping for noise reduction
  - Programmable gain and BW

The Data Handling Processor (DHP)



- One-to-one mapped to the DCD
- Data processing steps:
  - *Pedestal correction* → the signal offset due to pedestal, periodically determined, is stored in the DHP
  - *Common mode correction* → signal offset found in all raw data values sampled at the same time
  - Data reduction using the *zero suppression* → the pedestal and common mode corrected values are compared to a programmable threshold → only real data are transmitted
  - *Triggered readout scheme* introduces further data reduction
  - Control signal for the other ASICs

The readout electronics



- FLEX kapton cable 49 cm long
- Patch Panel (PP) for power filtering and impedance matching
- Data Handling Hybrid (DHH) for interconnection of the half-ladder to the outside world →
  - Clock signal from the BELLE II environment
  - Slow control master for the ASICs
  - Multiplexing data from DHP into optical link
- Compute Nodes (CN) – ATCA/ONSEN for tracking information from the SVD and definition of ROI within the PXD data

Self supporting all-silicon module

3D Model of Belle-II Ladder

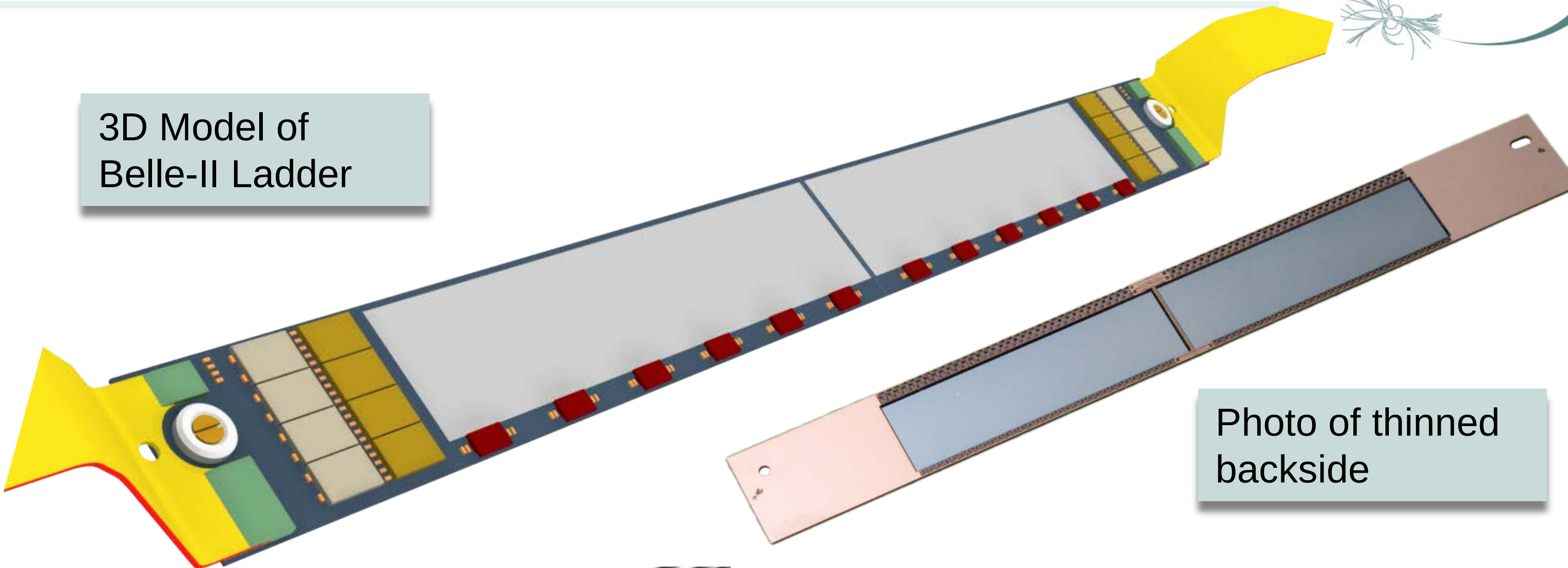
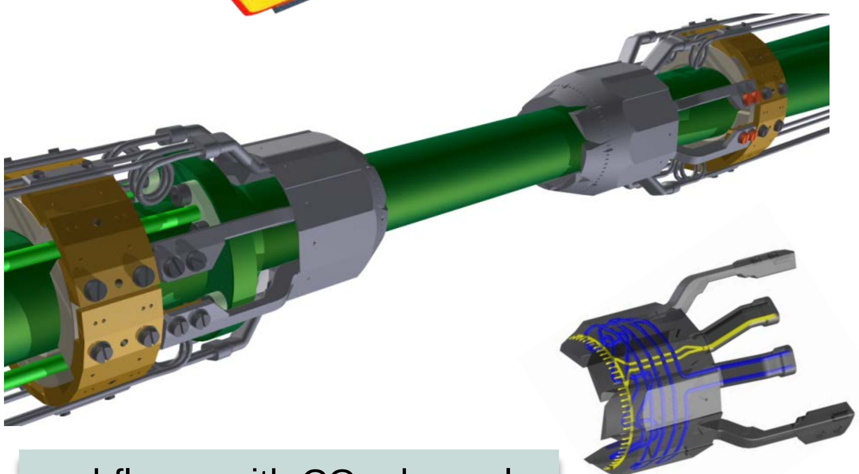
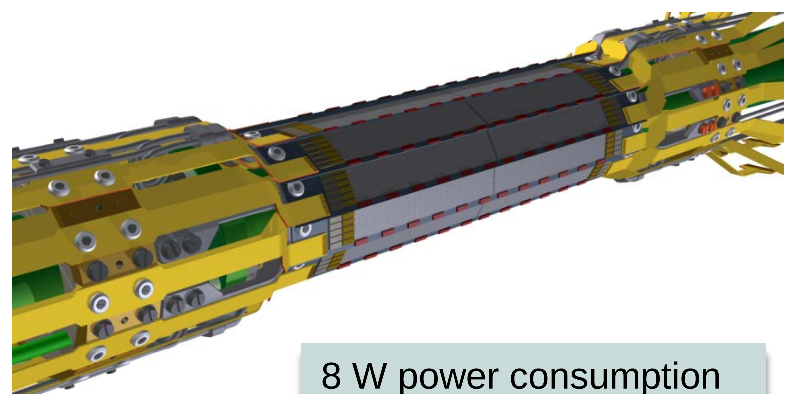


Photo of thinned backside

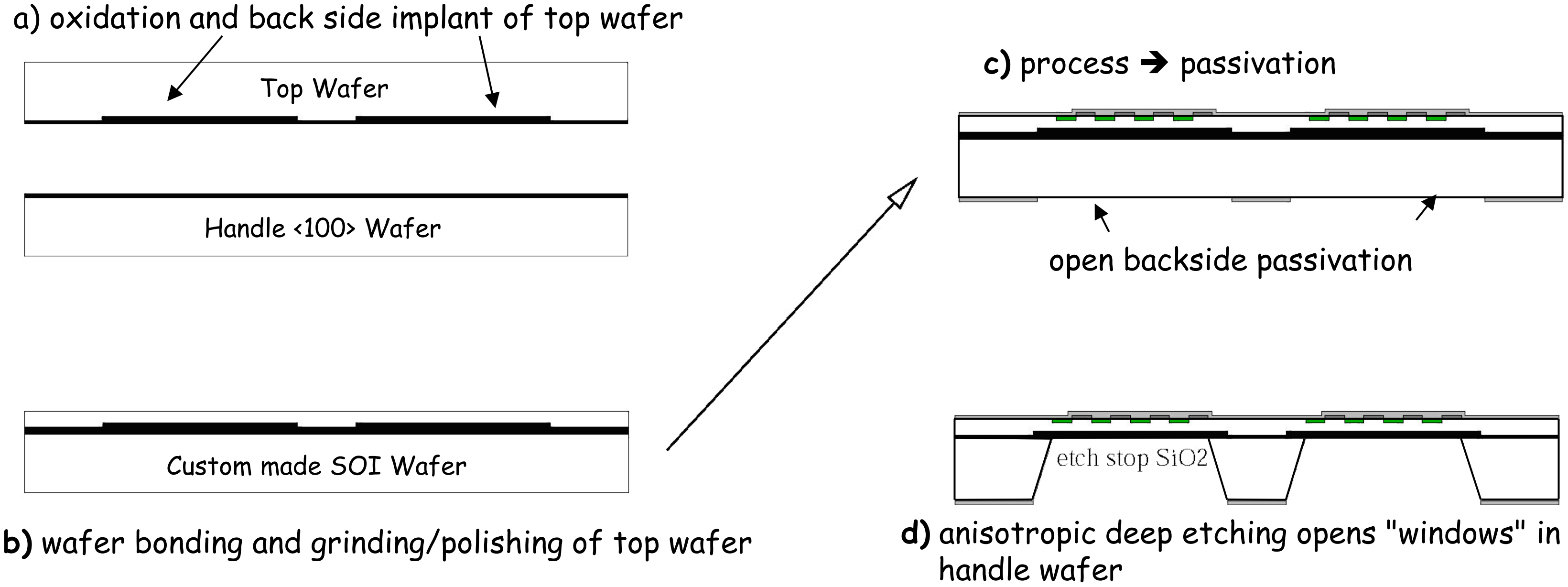


end-flange with CO_2 channels and capillaries for air cooling



8 W power consumption per half ladder, including 1 W from the sensor

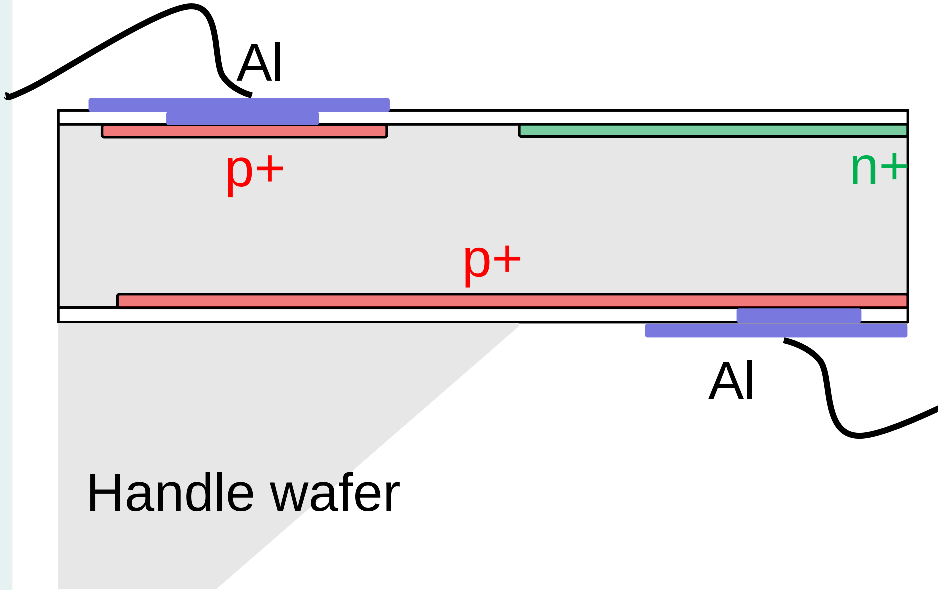
The DEPFET thinning technology

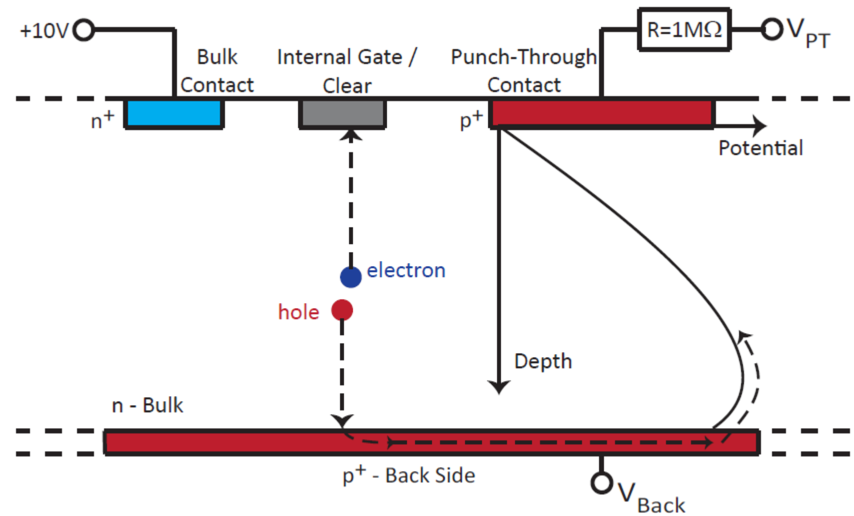


- Wafer bonding and thinning of top layer
- Sensor fabrication on SOI
- Etching of the handle wafer
- In house technology

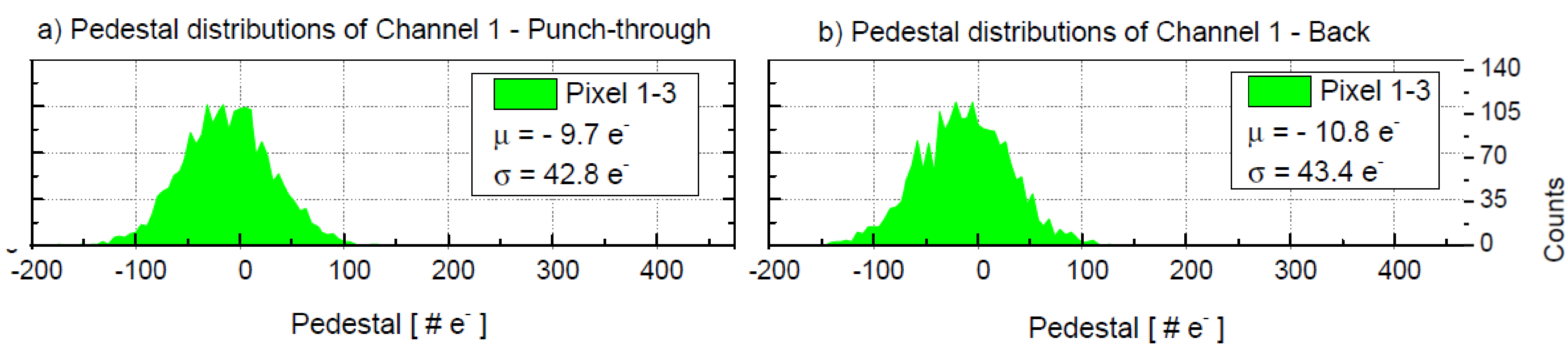
→ The **DEPFET thickness is hence a free parameter** which can be adjusted depending on the needs of the experiment → in BELLE II **0.2% X_0** of the full detector

Punch-through biasing of DEPFET

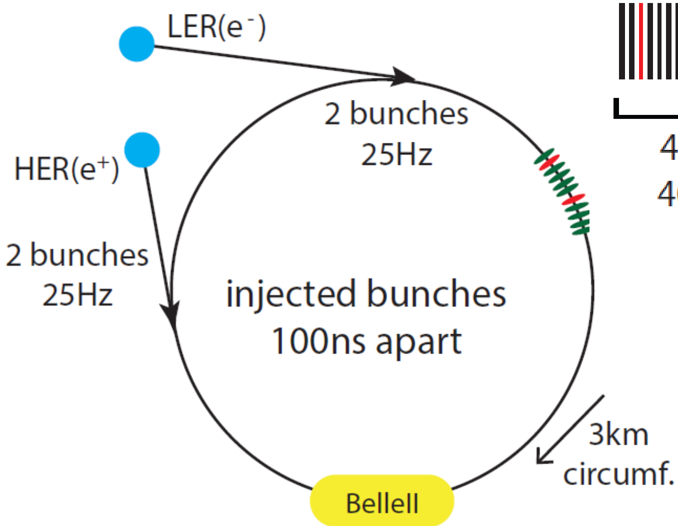


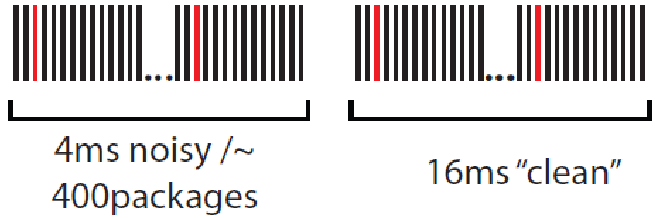


Simplification of the backside processing → no wire bonds on thin Si

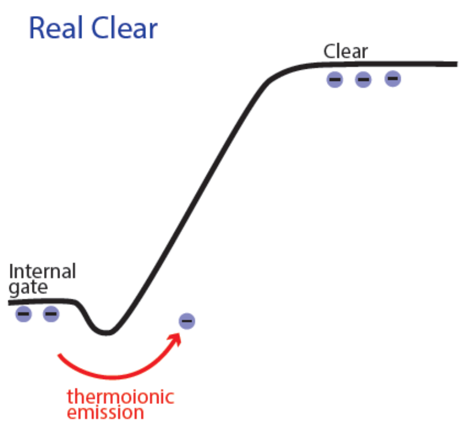


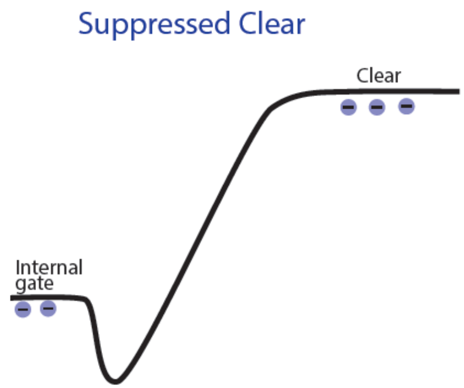
Gated mode operation of DEPFET matrix
(intrinsic electronic shutter)

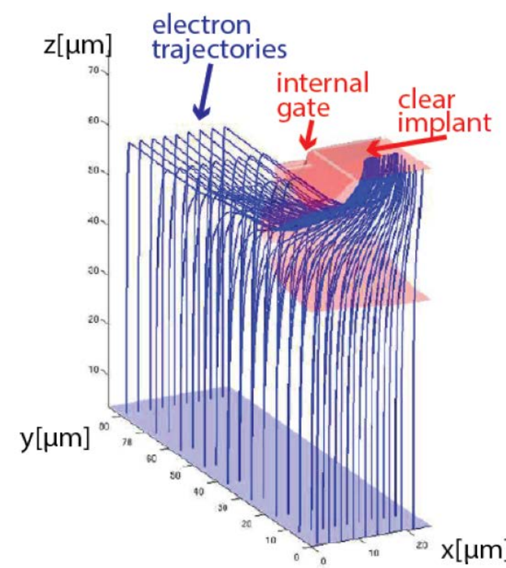




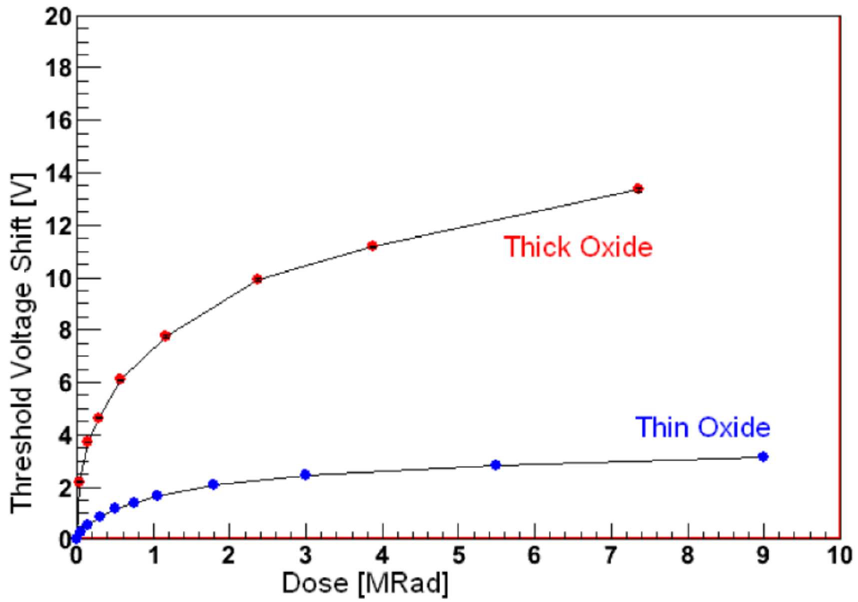
- Drain away electrons coming from noisy bunches
- Preserve electrons accumulated during "clean" bunches







Radiation damages in DEPFETs

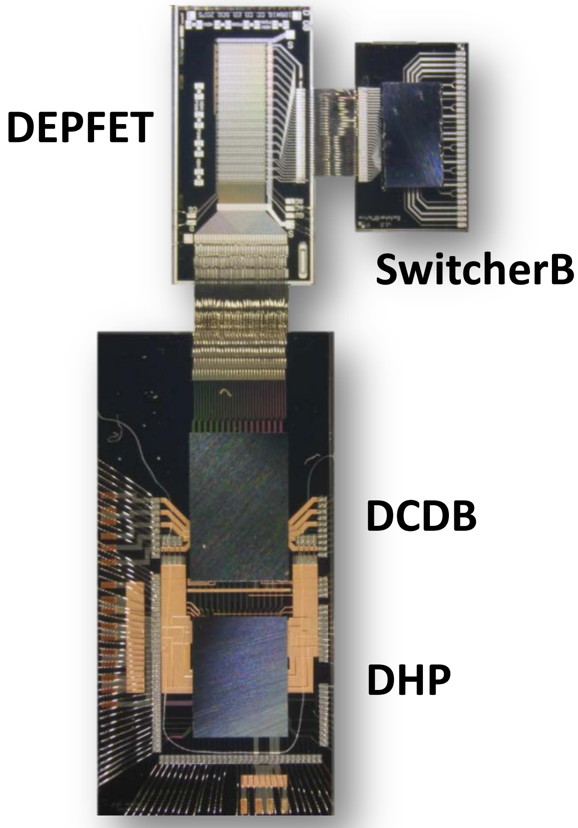


- The main cause of radiation damages in DEPFET detectors is due to *surface damages*

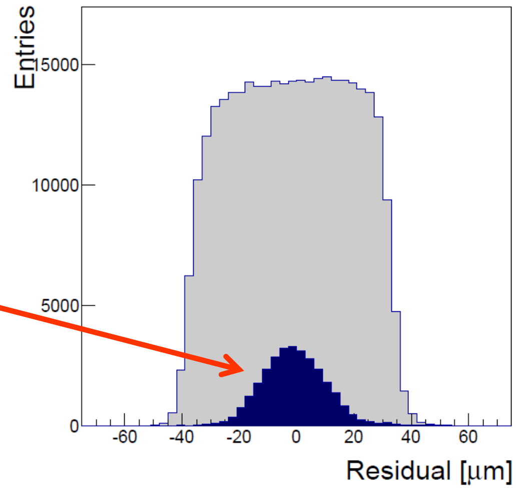
  → Increase of the threshold voltage → the electronics can cope with this!
- Bulk damages due to relatively low energy electrons could deteriorate the S/N → negligible effect

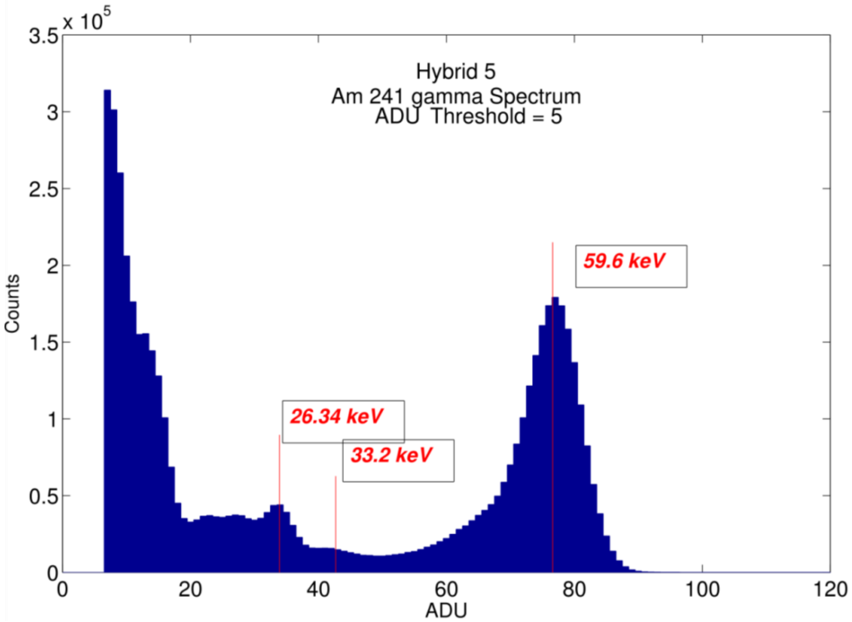
DEPFET pixelated detector proof of principle

- All the ASICs + Belle II DEPFET working together
- Trigger-less zero suppression readout
- Full speed operation (320 MHz)



$\sigma = 16\ \mu m$





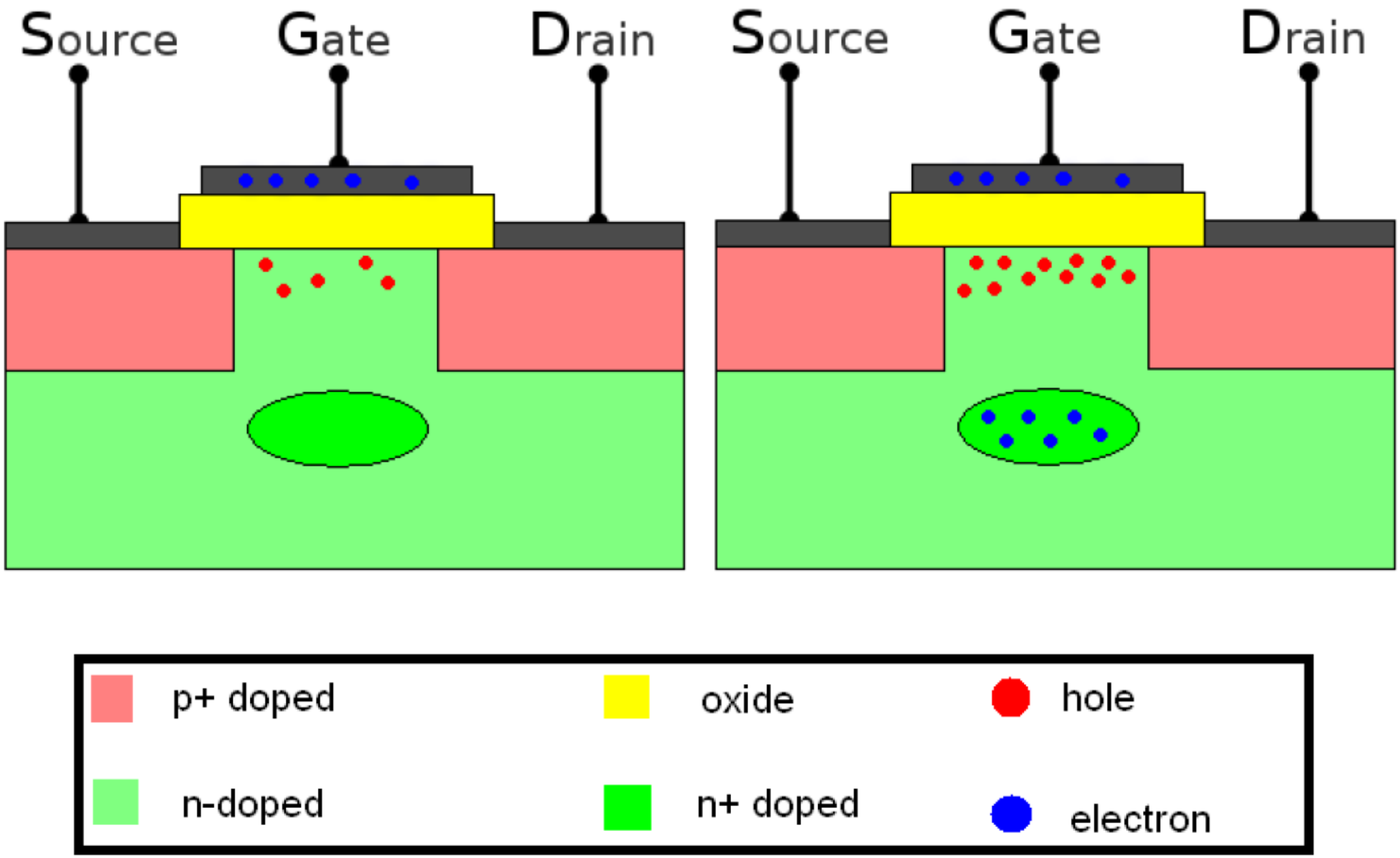
Summary

- The DEPFET PXD detector promises an excellent *spatial resolution* of ~ 15 μm and an *occupancy* as low as 1%, due to a fast readout (50kHz) and a huge number of pixels (~ 8Mpix);
- The *technology* used for the production of the DEPFET PXD is very complex and yet fully functional;
- The SOI technique allows building a full Silicon module and the control on *the thickness* of the DEPFET ladders, thinned down to 75 μm (0.2% X_0), minimising multiple scattering;
- The *power consumption* of a full sensor is ~ 3W in the acceptance region and can be easily handled with moderate air cooling;
- Considering the contribution from the readout electronics as well, the DEPFET PXD is characterised by a very high *SNR* of the order of 40;
- The DEPFET PXD has been proven to be *radiation tolerant* up to doses of the order of 10 Mrad.

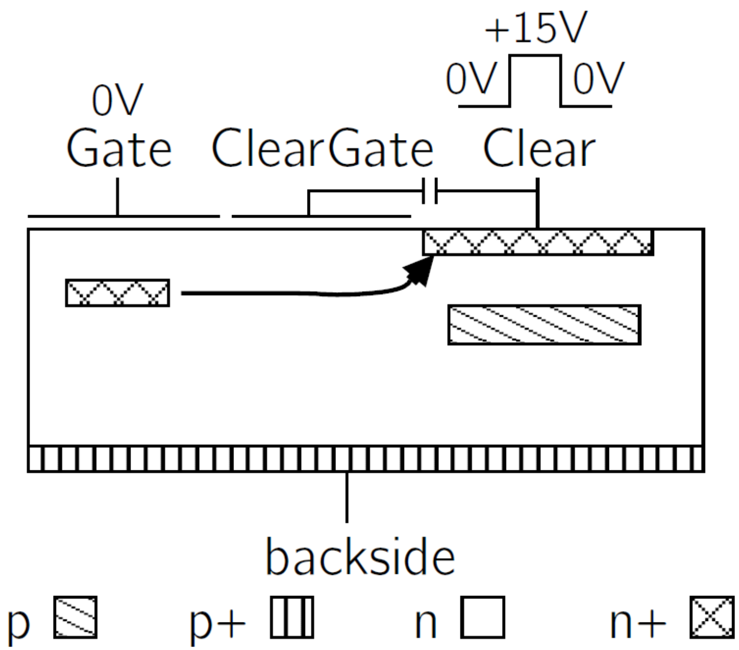
Thank you!

Backup slides

Charge collection in a DEPFET



The CLEAR mechanism



- The n^+ implant is a potential minimum for e^-
- The charge stored in the internal gate is removed applying a high positive voltage
- The e^- drift towards the clear contact and are then removed
- p-doped region used to shield the clear contact
- *Clear-gate structure* used to lower the potential barrier between the internal gate and the clear

The internal amplification and the readout methods

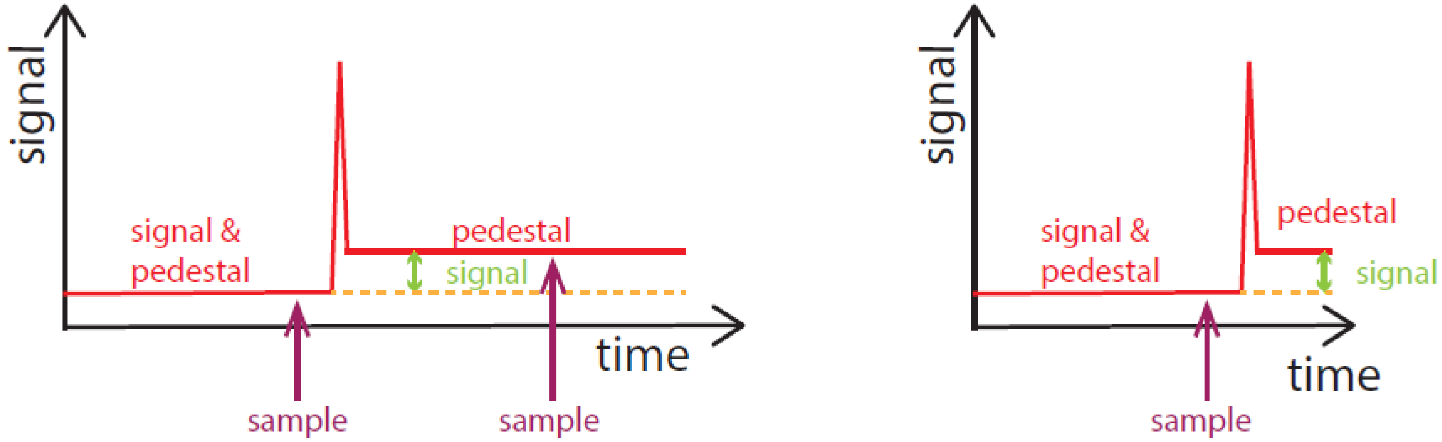
- The internal amplification g_q is defined as the increase in the drain current I_{ds} per e^- in the internal gate

$$g_q = \frac{\partial I_{ds}}{\partial Q_{sig}}$$

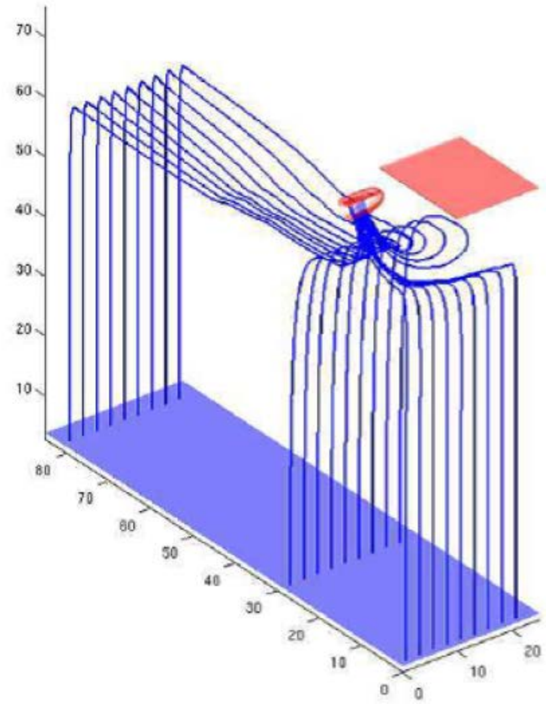
- I_{ds} increases linearly with Q_{sig}
- g_q and the transconductance g_m are proportional

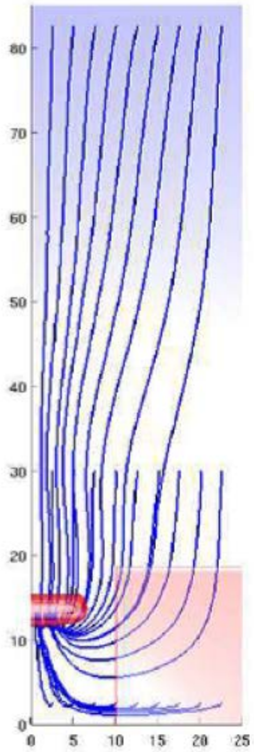
$$g_q = \frac{g_m}{C_{ox}}$$

- If I_{ped} is the current measured in absence of charges, the signal is given by $I_{sig} = I_{ds} - I_{ped}$



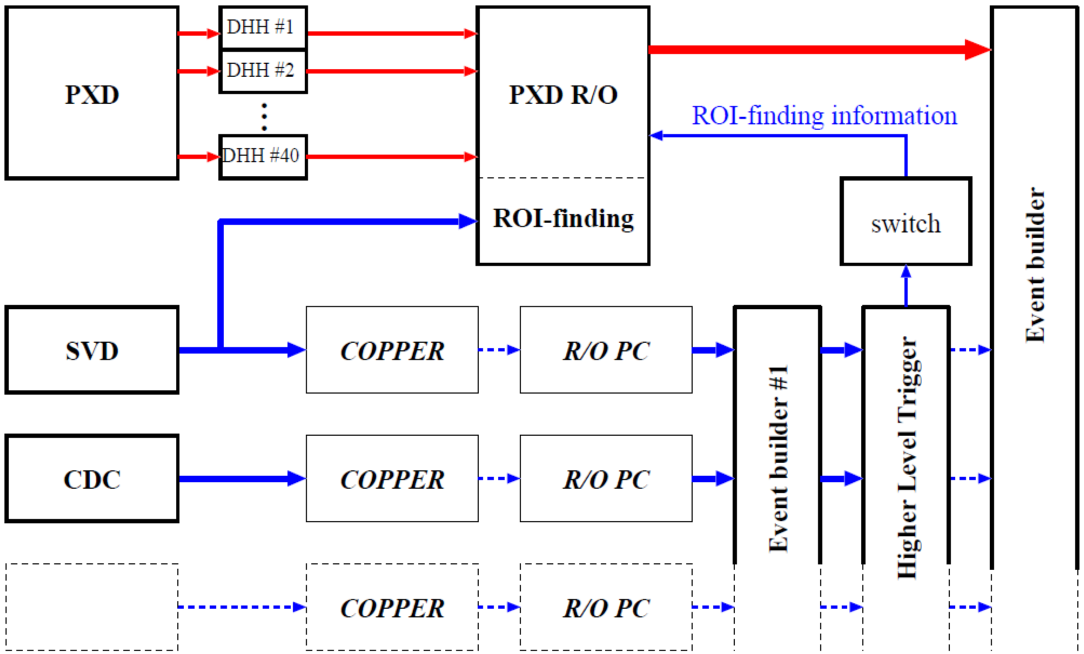
Electron trajectories within the DEPFET

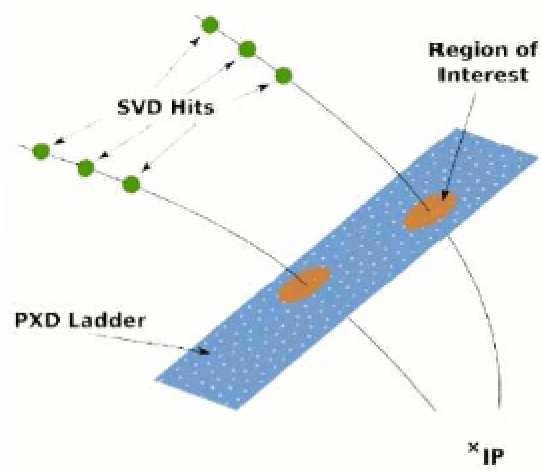




The readout chain: from the module to the outside world

- PXD sends ~7MB/event at 30kHz rate and 1% occupancy to DAQ
- A factor of 10 data reduction is performed using SVD
- A factor of 5 data reduction is performed using HLT





Noise reduction by track association: Only pixels inside the ROI will be stored (+ high energy deposition clusters)

Radiation damages

Surface damages

- Trapped oxide charge
  → shift of V_{thr} to negative values

- Interface traps :
  - Trapping of additional charges
    → V_{thr} to negative values
  - Degradation of charge carriers mobility in the channel
    → decrease of g_q

Bulk damages

- Formation of crystal defects (vacancies and interstitials) by PKA:
  - Increase of leakage current
    → degradation of S/N
  - Trapping/de-trapping of charge carriers
    → fluctuations in the depletion voltage
  - Change in effective doping